Coincidence Detector CD48

Eric Ayars, 2018

Specifications

- 4 inputs, internally selectable to either high-Z or 50-Ω impedance.
- 8 counters. Counters 0–6 are 24-bit counters (max 16,777,215), counter 7 is 16-bit (max 65,535.) Each counter can be configured to count coincidences for any combination of the 4 inputs. The maximum tested count rate is 10MHz.
- USB interface. The interface provides power to the device as well as allowing computer control and reporting. The devices appears on the USB bus as a virtual COM port under Windows, or equivalent under Linux/Macintosh. Communications (described below) are simple command-response pairs or —depending on setting— automatic count reporting at set intervals.
- Indicator lights: Each counter has an LED (labeled 0–7) to indicate activity on that channel. Each input has an LED indicating detection of a pulse larger than the trigger level. Error/Comm/Data LEDs indicate counter overflow, successful communications, and data send, respectively. (Comm LED is labeled 'Roger' on early boards.)
- Software-controlled DAC voltage output ranges from 0–4.08V on V/G pins. ('V' is erroneously labeled '7' on early boards.)
- Coincidence detection is edge-sensitive, and tested to be below ±30ns time resolution. (Typically 25ns.)
- Settings (other than VDAC output) are stored in EEPROM, so any time you plug this in it's pre-set to the last channel, level, input impedance, and repeat-time settings used.

Commands

C – Report counts on channels 0–7 and overflow status. Human-readable format.

c – Report channels 0–7, space-delimited, followed by overflow status. Not as human-readable, better for computer parsing.

E – Report and clear overflow flag. The overflow flag is an 8-bit register that describes which counter(s) have overflowed: bit 0 → counter 0, bit 7 → counter 7. An overflow value of 131, for example, would indicate that counters 2 and 7 have overflowed.

Counters 0–6 are 24-bit counters, so can count to 16,777,215. Due to hardware limitations, Counter 7 is limited to 16-bit operation, and can only count to 65,535. Should one expect this to be a problem, it is recommended that channel 7 be used for "rarer" coincidences.

H – Help (Prints much of this message.)

L*n* – Set input trigger level to n. n in this case is a byte (0–255) which maps to a range of 0–4.08V. (i.e. L127 sets trigger to 2.024V.) L sets an internal comparator reference voltage *above* which the incoming pulse is passed on to the rest of the analysis hardware. Depending on your noise level, setting L higher or lower may help discriminate against invalid signals.

P – Prints all settings: channel targets, repeat time, repeat status, trigger level, and impedance. This printout is in a nice human-readable format, appropriate for a terminal interface.

p – Reports channel settings in 4-bit (nibble) number, followed by repeat time, repeat status, trigger level, and impedance. Not as human-readable, better for computerized parsing. Settings are separated by spaces on a single return string.

r*n* – Sets repeat interval to n ms for reporting channel counts. i.e. 'r2000' → 2-second repeat. The minimum value of n is 100, the maximum is 65535. If n is given outside that range, the device sets to the upper or lower limit. For count periods larger than 65s, it's recommended to use use external control via 'C/c'.

R – Toggles repeat state. Off by default.

S*n***ABCD** – Set channel to desired inputs. n = channel number, ABCD = 1 or 0 for each input. i.e. 'S31010' sets counter 3 to watch A and C, not B or D.

T – Test: turn on all LEDs for 1s. This is included primarily as a quick test so we could see if we put the diodes in the right direction when we built the board.

Vn – Set output voltage to n. Note that n must be a byte, the actual voltage ranges linearly from 0-4.08 over a range of $n = 0$ to $n = 255$.

v – Return firmware version.

Z – Set input impedance high.

z – Set input impedance to 50 Ohms.

If a command is successful, the 'comm' light will blink in response. If the device could not parse the input, the command is ignored.

Test procedure

After assembly, each board was tested using the following procedure:

- Using a dual-channel digital function generator, send a square wave at $f = 100.000000$kHz into input A.
- With the same digital function generator, send a second wave at $f = 99.999900$kHz into B, C, and D.
- Set counters as follows:

Counter	A	B	C	D
0	1	0	0	0
1	0	1	0	0
2	0	0	1	0
3	0	0	0	1
4	1	1	0	0
5	1	0	1	0
6	1	0	0	1
7	0	1	1	1

- Since the difference in period between the two waveforms is $\Delta T = 10$ps, every 10 seconds the two waves will overlap and register coincidences. The *number* of coincidences during this overlap event will give the time width of the overlap, which then tells us the resolution at a rate of 100 counts per nanosecond. Typical overlap counts range from 4800 to 5500, corresponding to pulse proximity of 24–28ns. The variation is primarily due to variation in RC values on the pulse-shaping network for each input. Boards with overlap counts greater than 6000 (30ns proximity) are rejected.